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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,314	07/17/2003	Bonnie I. Wang	015114-066800US	4343

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EXAMINER
CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,314	WANG ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-17-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because lines, numbers & letters in Figs. 1 and 3-4 are not uniformly thick and well defined, clean, durable, and black. 37 CFR 1.84(l). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 4 is objected to because of the following informalities:

In claim 4, "resistors" on line 6 appears to be --resistor--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Bergman et al. (US PAT No.6,605,958).

Regarding claim 1, Figs. 9 and 11 of Bergman et al teaches an integrated circuit comprising a differential impedance termination circuit (150 in Fig. 11), the differential

impedance termination circuit comprising: first resistors (160s on top and bottom coupled in series via 166/164) coupled in series; and a first transistor (166) coupled in series with the first resistors; and a first memory (136 in Fig. 9, D Flip-flop is a memory) coupled to a gate of the first transistor that is programmed to effect an impedance of the impedance termination circuit, the impedance termination circuit being coupled between first and second differential pins of the integrated circuit.

Regarding claims 2-3, Figs. 9 and 11 of Bergman et al. teaches the integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array and an application specific integrated circuit (implementation of the integrated circuit in an FPGA or an ASIC is merely intended use: a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).).

Regarding claim 4, Figs. 9 and 11 of Bergman et al. teaches the integrated circuit according to claim 1 further comprising a second transistor (166 of 150 situated in the middle in Fig. 11), a second memory (136 in Fig. 9) coupled to a gate of the second transistor that is programmed to effect an impedance of the impedance termination

circuit, a second resistor (160s) coupled in series with the second transistor, the second resistor and the second transistor being coupled in parallel with at least one of the first resistors when the second transistor is ON (when 166 is on 150s are in parallel).

Regarding claim 5, Figs. 9 and 11 of Bergman et al. teaches the integrated circuit according to claim 4 further comprising a third transistor (166 of 150 situated in the most left in Fig. 11), a third memory (136 in Fig. 9) coupled to a gate of the third transistor that is programmed to effect an impedance of the impedance termination circuit, a third resistor (160s) coupled in series with the third transistor, the third resistor and the third transistor being coupled in parallel with at least one of the first resistors when the third transistor is ON (when 166 is on 150s are in parallel).

Regarding claim 6, Figs. 9 and 11 of Bergman et al. teaches the integrated circuit according to claim 4 further comprising a third transistor (166 of 150 situated in the most left in Fig. 11) coupled in parallel with the second resistor (166 and 160s are in parallel across the inputs of differential amplifier), a third memory (136 in Fig. 9) coupled to a gate of the third transistor.

Regarding claim 7, Figs. 9 and 11 of Bergman et al. teaches the integrated circuit according to claim 1 further comprising a second transistor (166 of 150 situated in the middle in Fig. 11) coupled in parallel with the first transistor (166s are in parallel across

the inputs of differential amplifier), a second memory (136 in Fig. 9) coupled to a gate of the second transistor that is programmed to effect an impedance of termination circuit.

Regarding claim 8, Figs. 9 and 11 of Bergman et al. teaches the integrated circuit according to claim 1 further comprising a second transistor (166 of 150 situated in the middle in Fig. 11) coupled in parallel with one or more of the first resistors (166 and 160s are in parallel across the inputs of differential amplifier), a third transistor (166 of 150 situated in the most left) coupled in parallel with the second transistor (166s are in parallel across the inputs of differential amplifier); a third memory (136 in Fig. 9) coupled to a gate of the third transistor.

Regarding claim 9, Figs. 9 and 11 of Bergman et al. teaches the integrated circuit according to claim 1 further comprising a second transistor (166 of 150 situated in the middle in Fig. 11) coupled in parallel with one or more of the first resistors and the first transistor (166 and 160s are in parallel across the inputs of differential amplifier), a second memory (136 in Fig. 9) coupled to a gate of the second transistor that is programmed to effect an impedance of the impedance termination circuit; second resistors (160s) coupled in series with the second transistor; a third transistor (166 of 150 situated on the most left) coupled in parallel with one or more of the second transistors and a third memory (136 in Fig. 9) coupled to a gate of the third transistor.

The method claims 10-19 are essentially the same as the rejected apparatus claims 1-9 and similarly are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

September 29, 2004